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The design of Delay Pulse Circuit for Ultrasonic Phased Array System

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ABSTRACT

This paper presents the development of delay pulse circuit with 1ns resolution for both driving ultrasonic array transducers and digital receive beamforming for ultrasonic phased array system. The circuit which can supply pulses with a 1ns time resolution employs the phase shifting with phase locked loop (PLL). In this way, 6 phase clocks with 1ns phase difference are generated, which are used to drive channel counters. Delay pulses of each channel are generated by counter. Based on this circuit, a design of digital receive beamforming with 1ns delay resolution is also presented. The design adopts a phase shifting technique of PLL to generate six clocks with 6ns periods and 1ns phase difference, which are selected as a non-uniform sampling clock to drive the A/D Converters according to the receive focal points. The delay pulse circuit is built with low-cast Field-programmable-gate-array (FPGA) components. By employing the novel architecture, the circuit has been achieved in FPGA. The simulation results are compared with two programmable delay chips and show that the proposed architecture achieves satisfactory performance for pulse delay.

INSTRUCTION

Simple ultrasound systems use a single large piezoelectric transducer to generate and receive ultrasound. However, state of the art systems use phased array technology similar to that used in contemporary radar and sonar. These systems use transducer arrays comprising a multitude of small transducer elements. Ultrasonic phased array techniques have been used in modem medicine in 1960s and extensively used in industry for NDT in 1980s[1,2,3,4].

High resolution beam focusing is achieved by pulsing the elements of an ultrasonic phased array transducer in some predetermined manner. In order to provide good focusing and a wide sweep angle for imaging purposes in non-destructive testing, the delays between pulses must be controlled to a fraction of the ultrasonic period. An ultrasound waveform is first generated and transmitted by exciting a piezoelectric transducer with a suitable electric signal. Pulses are delivered to the array elements in such an order that a composite wave front converges at a point. The distance and sweep angle of the point is determined by the timing of the pulses. This transmitted ultrasound beam propagates through tissue, undergoing diffraction and attenuation as well as scattering and reflection at tissue interfaces. Next, the reflected or scattered echoes propagate back to the transducer where they are received and converted to electric signals. These received echoes are then processed and mapped to form an image. In reconstruction of phased array ultrasound images, the imaging plane is scanned by beamforming-electronically steering and focuses the array both in transmit and receive modes. In the transmit mode, the beamforming process is performed at per scan angle. While in the receive mode, it is dynamically repeated for every image point[5,6]. Design of the transmit beamforming circuitry is relatively easy, since each transducer can be fired by digital timing, while design of the receive beamforming circuitry is an involved task and has been the subject of considerable research [7,8,9].

Conventionally, analog lumped L-C delay lines and programmable silicon delay lines have been used for delay compensation. For dynamic focusing, however, such imaging systems need a large number of delay taps and complicated programmable multiplexing circuitry. In addition to the system complexity, the hardware of delay lines is bulky and expensive. In the present high-frequency application, a 1ns timing resolution was deemed appropriate. It is, of course, perfectly possible to use programmable down counters to produce digitally controlled pulsed. The counter is loaded with a delay value, and then clocked until the terminal count is reached. However, to achieve a 1ns time resolution, a 1-GHz clock must be used. This would require high-speed, high-power technologies and also increase the cost[10].

Receive beamforming can also be carried out using conventional analog imaging methods, in which tapped L-C delay lines are commonly used for delay compensation. Figure 1 (a) shows the symbolic representation of analog phased array receive beamforming. In an analog delay system, a large number of delay taps are required for dynamic focusing, which results in complicated multiplexing and control circuits with high parts counts. Besides the system complexity, signal distortion at the output of analog delay circuits is caused by switching transients and the inherent artifacts of L-C delay devices such as insertion loss and impedance mismatching because the delayed signals are selected at different tap positions for different imaging points.

In the digital receive beamforming, the amount of delay can be split into an integer multiple and a fractional part of the

sampling period by using uniform sampling clock. While the integer part of the delay can be implemented with a memory delay line, the fractional part can be realized by interpolation filtering. This scheme is basically depicted in, see Figure 1(b). The samples from all channels are stacked in FIFO registers at each channel for synchronization, and then all of them are added[11,12,13,14,15]. Although digital dynamic focus method has been successfully used in conventional phased array imaging, there remain some practical difficulties to implement the digital beamforming system. In most conventional digital focusing systems, pulse echoes received at array elements are sampled synchronously by the same uniform sampling clock. A high sampling rate is required to obtain finely delayed samples. In addition, the digital beamforming hardware is complex, being dependent on the sampling rate and the number of array elements. As the sampling rate increases in a digital beamformer, larger and faster digital memories are required, and accordingly, the addressing circuit on these memories becomes more complex.

Figure 1(c) shows the scheme of receive beamforming by a non-uniform sampling clock of the A/D converter. In order to provide good beamforming, the delays must be controlled to a fraction of the ultrasonic period. In the present high-frequency application, a 1ns timing resolution was deemed appropriate. However, to achieve a 1ns time resolution, a 1-GHz clock must be used. This also require high-speed, high-power technologies and increase the cost.

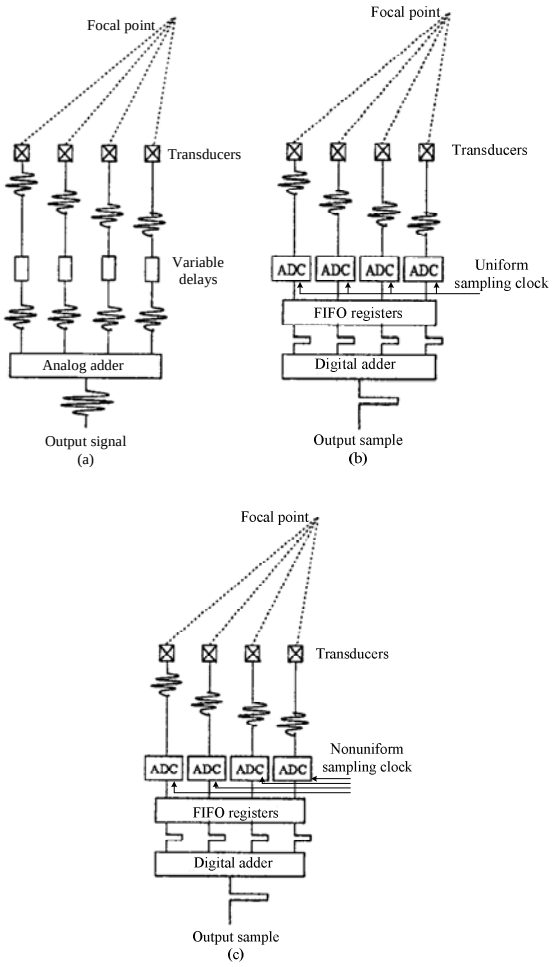

Figure 1. The symbolic representation of phased array receive beamforming by a) analog b) uniform sampling clock c) non-uniform sampling clock

This paper presents architecture of delay pulse circuit for both transmit and receive beamformer. Instead of using a single high-speed clock and analog or digital delay lines to meet the resolution requirements, the design employs the phase shifting with phase locked loop (PLL) which is built in FPGA chips.

ARCHITECTURE OF THE 1NS RESOLUTION DELAY PULSE CIRCUIT

The FPGA chips chosen for realization of the delay pulse circuit have the follow features: one is shortest delays of intrinsic gates and interconnections, and the other is an appropriate granularity and functionality of the basic logic blocks. The PLL which is built in FPGA chips has advanced clock shift capability to provide programmable phase shifting.

The present logic structure is shown in Figure2. As 25MHz clock signal (clk_25MHz) inputs PLL, the three clock signals with a period of 6 ns are derived. They are clk_out[0] (with 0 ^{o} phase shift), clk_out[1] (with 60^{o} phase shift) and clk_out[2] (with 120^{o} phase shift) respectively. By inverting each of them, three clock signals with a period of 6 ns are derived. They are clk_out[3] (with 180^{o} phase shift), clk_out[4] (with 240^{o} phase shift) and clk_out[5] (with 120^{o} phase shift) respectively. To achieve a 1ns time resolution, each of the six clock signals clk_out[0,…,5] has a period of 6ns but separated by 1ns from each other. In this way, 1ns time resolution is obtained using PLL and inverters.

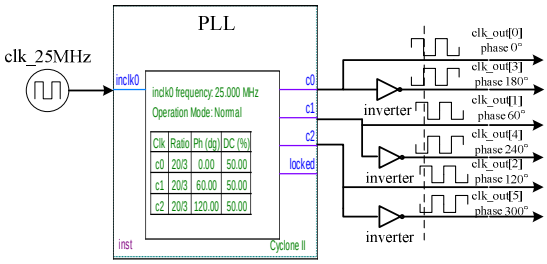

Figure 2. The FPGA delay pulse circuit with 1ns resolution

ARCHITECTURE OF THE TRANSMIT DELAY CIRCUIT

In order to generate trigger pulse with 1ns resolution, a combination of coarse and fine delay strategy is adapted. The coarse delay is the integer multiples of the clock periods. And coarse delay value is loaded in a 16-bit counter of which there is one per pulse channel. The fine delay is obtained by selecting from one of six shifted clocks. By means of a 6-to-1 clock multiplexer, the appropriate counter clock is selected to give 1ns resolution.

The design has been implemented by utilizing the FPGA chip. The FPGA chip is implemented using ALTERA device from the Cyclone family: EP2C5F256 in a 256pin BGA package. Cyclone II PLLs offer phase shifting and have three clock outputs. The simulation and programming tasks were accomplished with the aid of the “Quartus II” software provided by the manufacturer Altera.

The timing diagram of delay pulse circuit is shown in Figure 3. Clk_25MHz is the input clock of PLL. Trigger_in is SYNC signal which starts the process of transmission

Clk_out[0,…,5] are shifting clocks with 6ns of period and 1ns from each other. Trigger_clk[0,…,7] are 8-channel trigger pulses which drive 8 ultrasonic array transducers.

The timing diagram of trigger pulses is shown in Figure 4. 8 channels of trigger pulses are simulated. The range of delay time of each them is 0~255ns and the step increment is 1ns. The total data is 2048(8×256=2048). The delay time is relative to SYNC signal. The tolerances of delay change per step is ±0.16 and max deviation from programmed delay is ±0.38.The parameters of present scheme are compared with 3D7408-1* and DS1020-100** which are programmable delay line chips in Tabel 1.

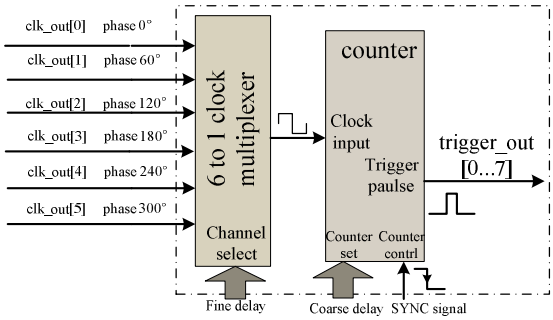

Figure 3. The logic structure of the implemented transmit delay pulse

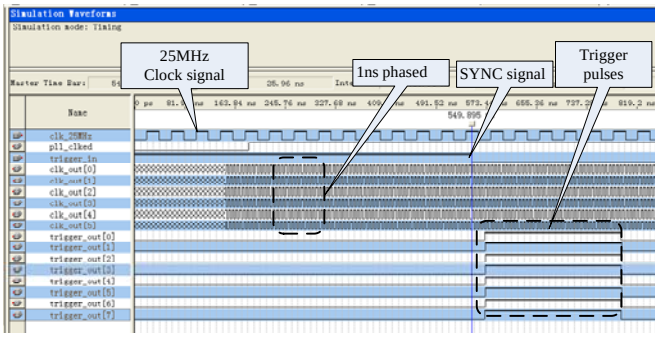

Figure4. The timing diagram of delay pulse circuit

Table 1. Delays and tolerances(in ns)

Model	Step zero delay time	Delay change per step	Max deviation from programmed delay
3D7408-1	12±2	1.00± 0.50	±5.0
DS1020-100	10±2	1*	±20
Proposed design	8.34±0.16	1±0.32	±0.38

Notes Not indicated in data sheet*

ARCHITECTURE OF THE RECEIVE BEAMFORMING DELAY CIRCUIT

The beamforming logic structure is shown as Figure 5. Instead of using a single high-speed clock to meet the resolution requirements, the design employs the phase shifting with the phase locked loop (PLL) which is built in the FPGA chips. The coarse delay is the integer multiples of the clock periods and the fine delay is obtained by selecting from one of six shifted clock signals. Sample clock of A/D converter is produced by 1/4 frequency divider, and the sampling rate is 24ns per period (41.7MHz). Analog signals are sampled by non-uniform sampling clocks and stored at each FIFO registers and then summed to produce the output sample.

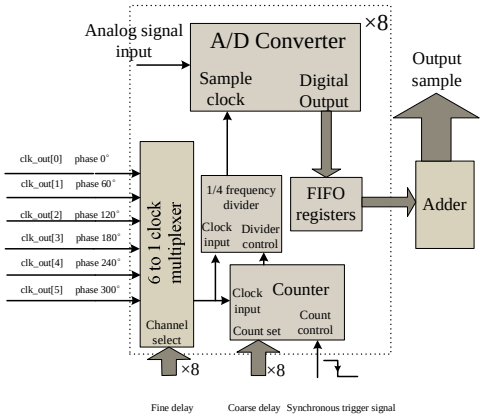

Figure 5. The logic structure of the implemented receive beamforming

Preliminary experiments were carried out with a FPGA chip and 8 A/D Converters. The simulation and programming tasks were accomplished with the aid of the "Quartus II" software provided by the manufacturer Altera. Because A/D converting technology, FIFO and Adder are well-performed, the generation of non-uniform sampling clocks is mainly considered.

The receive beamforming uses Altera Cyclone II FPGA chip (EP2C5F256). Cyclone II PLLs offer phase shifting and have three clock outputs. Non-uniform sampling clock of an individual channel is applied using a combination of coarse and fine delays. The coarse delays are integer multiples of the clock signal, and fine delays are applied with selecting channel of 6 to 1 clock multiplexer.

The timing diagram of sampling clocks is shown in Figure 6. Clk_25MHz is the input clock of PLL. Trigger_in is synchronous trigger signal which starts the process of receive beamforming. Clk_out[0,…,5] are shifting clocks with 6ns of period and 1ns from each other. Sample_clk[0,…,7] are non-uniform sampling clocks which drive A/D converters.

8 non-uniform sampling clocks are simulated. The range of delay time of each of them is 0~255ns and the step increment is 1ns. The total data is 2048(8×256=2048). The delay time is relative to the synchronous trigger signal. The tolerances of delay change per step is ±0.14 and max deviation from programmed delay is ±0.34.The parameters of the present scheme are compared with 3D7408-1 and DS1020-100. The results are shown in Table 2.

* http://www.datadelay.com/datasheets/3d7408.pdf

** http://pdfserv.maxim-ic.com/en/ds/DS1020.pdf

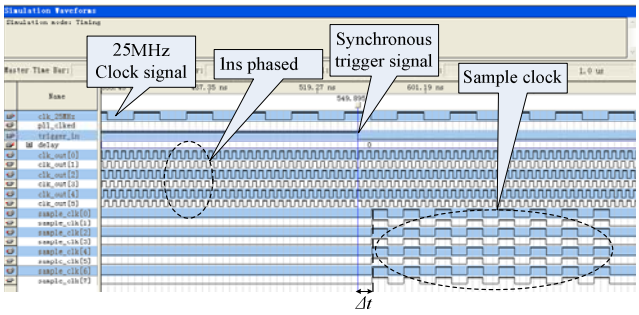

Figure 6. The logic structure of the implemented receive beamforming

Table 2. Delays and tolerances(in ns)

Model	Step zero delay time	Delay change per step	Max deviation from programmed delay
3D7408-1	12±2	1.00±0.50	±5.0
DS1020-100	10±2	1*	±20
Proposed design	6.7±0.14	1.00±0.14	±0.34

Notes* Not indicated in data sheet

CONCLUSION

The design of delay pulse circuit to drive ultrasonic array transducers is proposed. The hardware is built with FPGA. The specified time resolution of 1ns has been met. And the results of test of the design are compared with several programmable delay chips and have demonstrated that high delay with 1ns resolution can be produced using the presented design.

An architecture of receive beamforming for ultrasonic phased array system is also proposed. The generation of non-uniform sampling clocks is considered. For convenience, other blocks such as A/D converters, FIFO registers and Adder are not discussed because they are common to any phased array system. The results of the test of the design are compared with two programmable delay chips and have demonstrated that high delay with 1ns resolution can be produced using the presented design.

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